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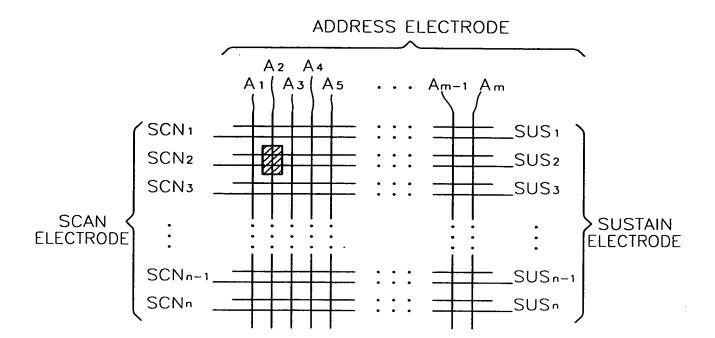
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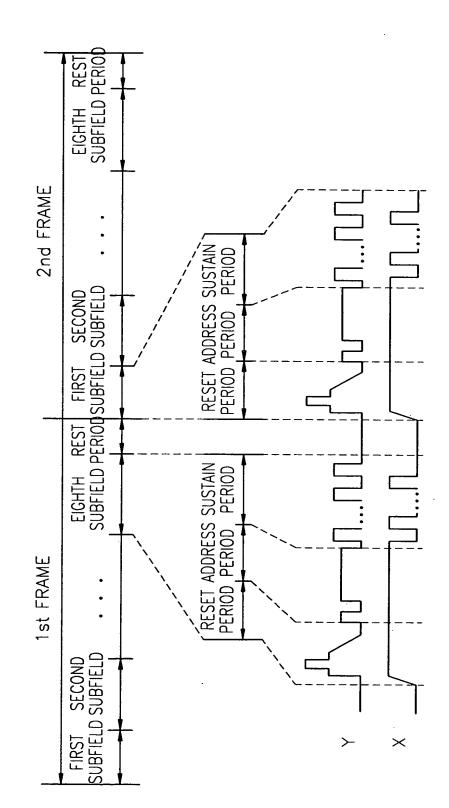
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FIG. 2

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FIG. 4A

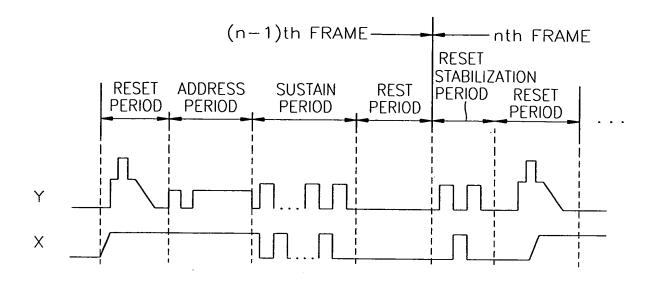


FIG. 4B

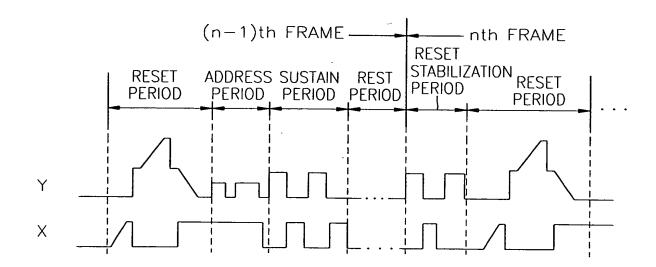
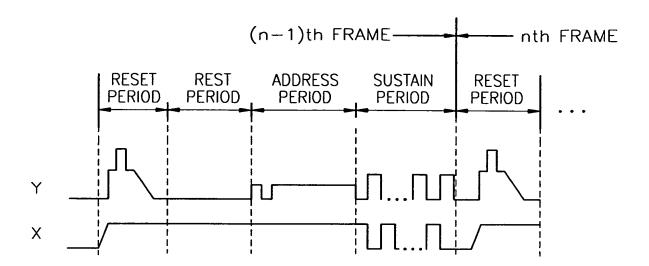


FIG. 5



65 X DRIVE PANEL 67 Y DRIVE 99 SIGNAL SYNTHESIZING CIRCUIT 645 642 643 644 64 RESET PULSE GENERATOR ADDRESS PULSE GENERATOR SUSTAIN PULSE GENERATOR SCANNING CIRCUIT TIMING FRAME GENERATOR 62 63 FRAME MEMORY 61

FIG. 6

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FIG. 7

